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Electrical Test Structures for the Characterisation of Optical Proximity Correction

Andreas Tsiamis^a, Stewart Smith^a, Martin McCallum^b, Andrew C. Hourd^c,
J. Tom M. Stevenson^a and Anthony J. Walton^a

^aInstitute of Integrated Micro and Nano Systems, School of Engineering and Electronics,
Scottish Microelectronics Centre, The University of Edinburgh,
Kings Buildings, Edinburgh, EH9 3JF, UK;

^bNikon Precision Europe GmbH, Appleton Place, Appleton Parkway,
Livingston, West Lothian, EH54 7EZ, UK;

^cCompugraphics International Ltd., Eastfield Industrial Estate,
Glenrothes, Fife, KY7 4NT, UK

ABSTRACT

Simple electrical test structures have been designed that will allow the characterisation of corner serif forms of optical proximity correction. The structures measure the resistance of a short length of conducting track with a right angled corner. Varying amounts of OPC can be applied to the outer and inner corners of the feature and the effect on the resistance of the track measured. These structures have been simulated and the results are presented in this paper. In addition a preliminary test mask has been fabricated which has test structures suitable for on-mask electrical measurement. Measurement results from these structures are also presented. Furthermore structures have been characterised using an optical microscope, a dedicated optical mask metrology system, an AFM scanner and finally a FIB system. In the future the test mask will be used to print the structures using a step and scan lithography tool so that they can be measured on-wafer. Correlation of the mask and wafer results will provide a great deal of information about the effects of OPC at the CAD level and the impact on the final printed features.

Keywords: Mask Metrology, Optical Proximity Correction, Electrical Measurement

1. INTRODUCTION AND BACKGROUND

The work presented here forms part of an ongoing project investigating the application of electrical metrology techniques, normally associated with microelectronics, to the measurement of advanced photomasks. Previous publications¹⁻⁷ have demonstrated the capability of on-mask electrical measurements of Critical Dimensions (CD) to be faster and more repeatable than traditional techniques. This is especially true for masks using strong phase shift techniques where optical and CD-SEM measurements are affected by the presence of phase shifting features.

The electrical CD measurements are based on test structures which allow the measurement of the sheet resistance of conducting films, which is then used to calculate the width of a resistor of known length from the measured resistance. The test structure used to measure sheet resistance (R_S) is a special case of a “van der Pauw” four terminal sheet resistor known as a Greek cross.⁸⁻¹¹ The linewidth test structure is a Kelvin connected bridge resistor. This has four terminals, two used to force current and two used to sense the voltage drop along a known length of conducting track. Because the voltage and current terminals are separate the measured resistance does not include contact resistances or effects from the measurement equipment. The measured resistance can be used, along with the sheet resistance of the material and the length of the bridge, to calculate the average Electrical Critical Dimension (ECD).^{12,13}

Further author information: (Send correspondence to A.T.)
A.T.: E-mail: A.Tsiamis@ed.ac.uk, Telephone: +44 (131) 650 5623

On-mask electrical measurements of ECD have been made using test structures fabricated in the chromium light blocking layer of a standard chrome-on-quartz photomask plate. These have been used in previous publications to examine the effects of the proximity and alternating aperture phase shifting fabrication on CD.¹⁻⁷ The results of ECD measurement have been shown to compare very favourably with traditional mask metrology methods, especially for deep sub-micron dimensions. This information could be used, for example, to create models of one dimensional proximity effects for the correction or biasing of feature sizes without the confounding influence of proximity effects associated with light and electron optical metrology tools.

The present work attempts to extend the earlier ECD measurements to two-dimensional OPC features,¹⁴ in particular the characterisation of corner serifs. The corner serif is found with increasing frequency on advanced mask designs and presents a particular challenge to conventional metrology techniques.¹⁵ This is even more relevant where less than ideal image rendering and over-aggressive design may lead to serif features becoming “pinched off” from the main corner feature. Electrical techniques should be suited to detecting these abnormalities, particularly on inner corner serifs, and it is anticipated that it will be possible to relate these measurements to serif area as a means of metrology checking.

2. TEST STRUCTURES

The test structure design for this project is a Kelvin connected resistor consisting of a short section of metal track turning through a right angled corner, as shown in figure 1(a). In order to measure the resistance of the track a current is forced between pads B and D while the resulting potential difference is measured at pads A and C. The resistance of the section of track between the voltage taps is then

$$R = \frac{V_{AC}}{I_{BD}} \quad (1)$$

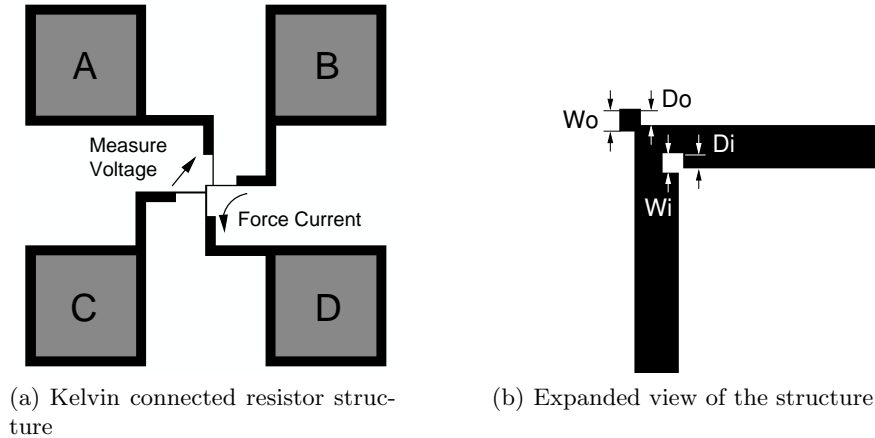


Figure 1. Layout of Kelvin test structure and closeup showing parameters of OPC features.

The effect of OPC is examined by altering the layout of the right angled corner of the structure. Specifically, a square of metal is added to the outside of the corner while a square is subtracted from the inside. This is illustrated in figure 1(b). The degree of OPC is altered by changing the size of the square (W_i and W_o) and the amount by which it overlaps with or protrudes from the original layout (D_i and D_o).

The test mask design has test structures with 3 different base values of CD: $1.6\mu\text{m}$, $2.0\mu\text{m}$ and $2.4\mu\text{m}$. These correspond to printed dimensions of 320nm, 400nm and 480nm when imaged with a 5X projection lithography tool. The dimensions of the OPC elements are defined as fractions of the base CD: 0.25, 0.3, 0.35, 0.4, 0.45 and 0.5. Subsequently, the value of D_i/D_o is then defined as some fraction of W_i/W_o : 0.25, 0.5 or 0.75. The test mask has the full range of OPC dimensions for the $1.6\mu\text{m}$ structures and a reduced set for the other CDs with only the D_i/D_o values defined as half of W_i/W_o .

3. SIMULATIONS

The two-dimensional (2D) solver of the interconnect analysis software *Raphael* was used to model the resistance of test structures with different levels of OPC applied either to the inner or the outer corner. Having the mask design as a starting point, simulations were performed on structures with OPC features in either or both the inside and outside corners. A sheet resistance of $22.5\Omega/\square$ was chosen for the material of the simulated structures, as this represents a typical value of the chrome layer, measured on previous masks. The results of the simulations for test structures with a base CD of 1600nm and serifs removed from the inner corners are presented in figure 2(a), while those for structures with serifs added to the outer corners can be seen in figure 2(b).

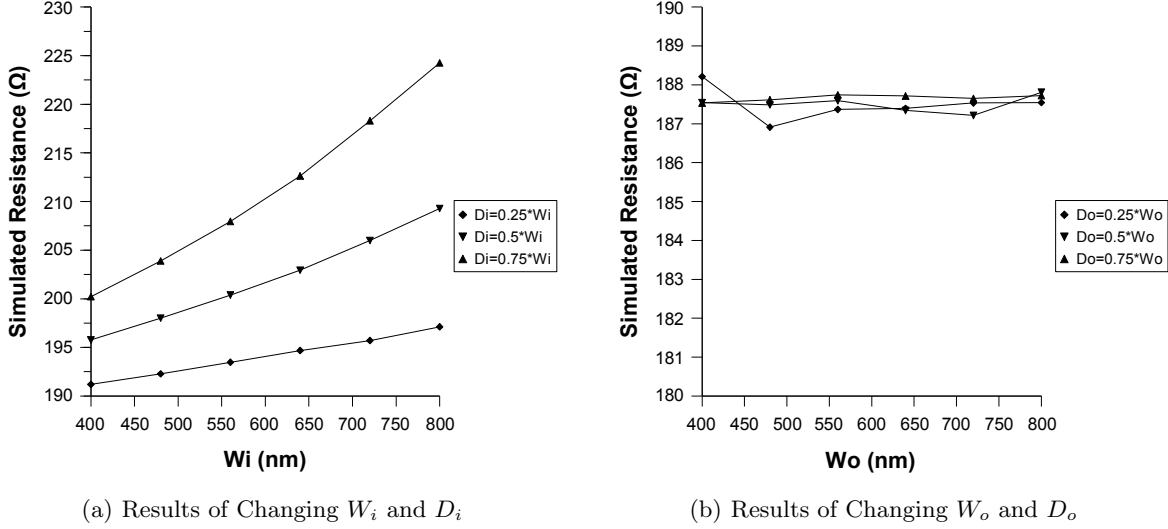


Figure 2. Simulation results showing the effects of changing the dimensions of the OPC features.

The results show that when the correction is applied to the inner corner there is a significant resistance change with respect to the dimensions of the OPC feature. In particular, it appears that the resistance strongly depends on the area of the material removed to form the serif in the structure. This behaviour is to be expected as most of the current flow in the structure is concentrated around the region of the inner corner. This is illustrated in figure 3 which shows a contour plot of the current density around the corner of a 1600nm wide structure with inner and outer serifs. There is little variation of resistance when the area of the outer serif changes and this is to be expected as there is little or no current flow in this region of the structure. Any resistance variation caused by altering the dimensions of the outer serif will be concealed by real mask effects (such as R_S and CD variations) that are not present in the simulations.

Finally, simulation results from 1600nm wide test structures with OPC features on both the inside and the outside corners are presented. Figure 4(a) shows the resistance values for structures where the inner serif dimensions vary while the the outer serif feature remains the same ($W_o = 0.25 \times \text{CD}$ and $D_o = 0.25 \times W_o$). Similarly, figure 4(b) shows the results for structures with varying outer serif dimensions and the same inner serif feature ($W_i = 0.25 \times \text{CD}$ and $D_i = 0.25 \times W_i$). It can be seen that the addition of an outer OPC feature will have little effect, certainly smaller than any resistance change associated with varying the inner serif dimensions. On the other hand the addition of an inner serif will change the resistance of a structure far more than any resistance variation caused by the alteration of the outer serif area.

4. ON-MASK MEASUREMENTS AND RESULTS

4.1. Electrical Measurements

On-mask electrical measurements on structures that match the simulations have been made on a binary test mask (MSN6754). This mask contains two blocks of on-mask test structures and one block of large pad printable

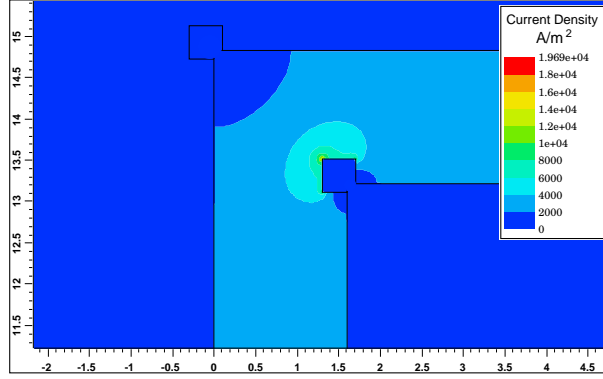


Figure 3. Current density scalar contour plot for a simulated corner structure with inner and outer serifs.

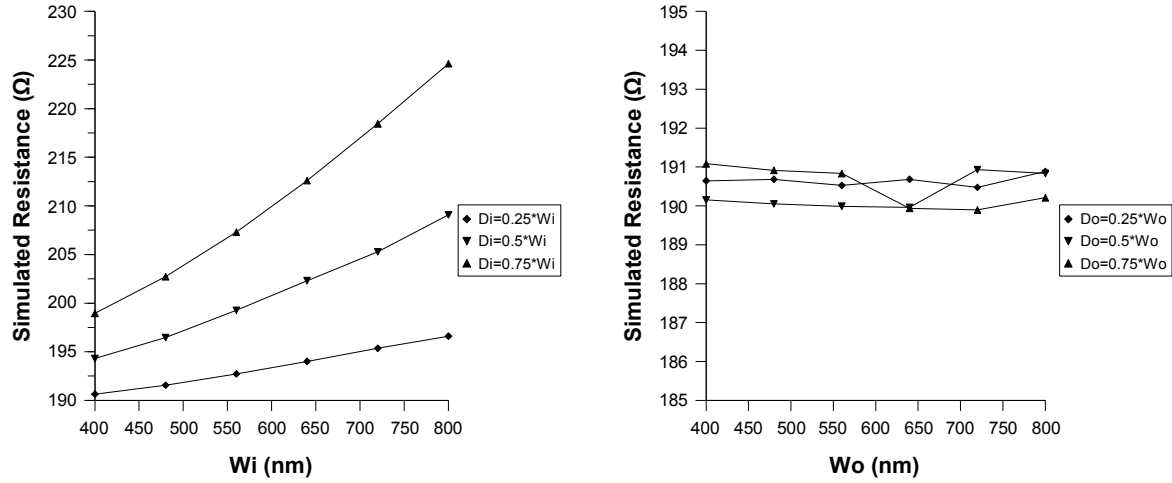
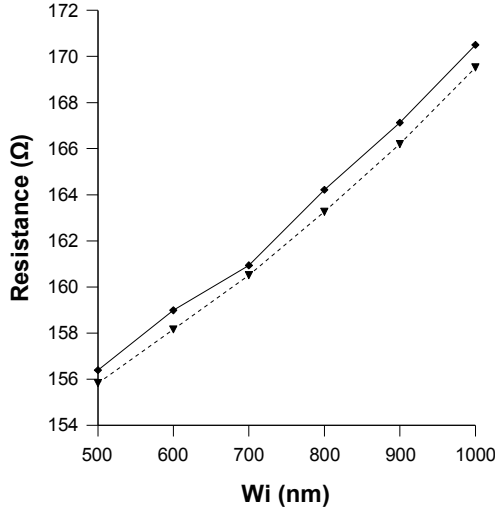


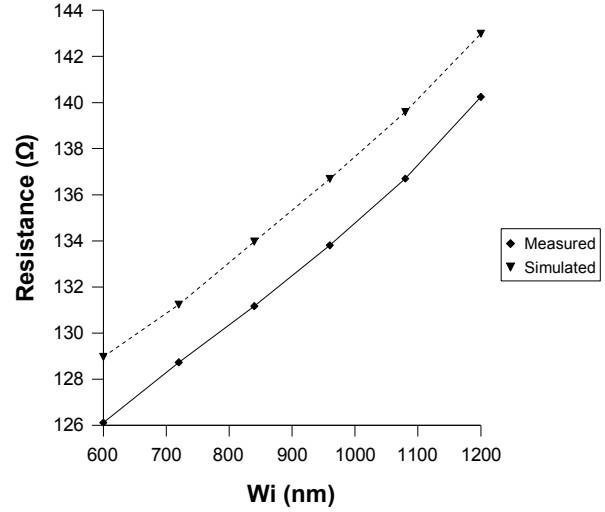
Figure 4. Simulation results showing the effects of changing the dimensions of the OPC features for structures with both inner and outer serifs.

test structures, designed to be measurable when reduced by a 5X photolithography system. Figures 5(a) and 5(b) show both the measured and simulated results for 2000nm and 2400nm wide structures with inner corner serifs and $D_i = 0.5 \times W_i$. These are part of the reduced sets, which have wider corner structures with larger OPC feature dimensions. The electrical measurements and simulation results are very similar, though the offset in resistance is obvious. This offset is most probably due to differences in the sheet resistance or CD. While the simulated structures use the design CD, for on-mask features there is usually a non-linear transfer between fabricated and nominal width. In fact the trend in the offset between measured and simulated resistance changes from positive to negative as the nominal CD increases, which suggests just that. In addition the simulations use a constant R_S value, while in reality there will be R_S variations from structure to structure (albeit small). Finally, there are differences between the slopes of the measured and simulated results which is likely to be caused by inconsistencies, such as corner rounding, between the geometry of the structures on the mask and the designed structure used in the simulations.

In any case, the presence of OPC shows the expected strong effect on the resistance of a conducting track when applied to the inside of a right angled corner but little effect when applied to the outside. The rate of change of measured resistance with inner corner serif size is sufficient to make an unambiguous relationship between the two parameters. This can be seen more clearly in figures 6(a) and 6(b), which present the results



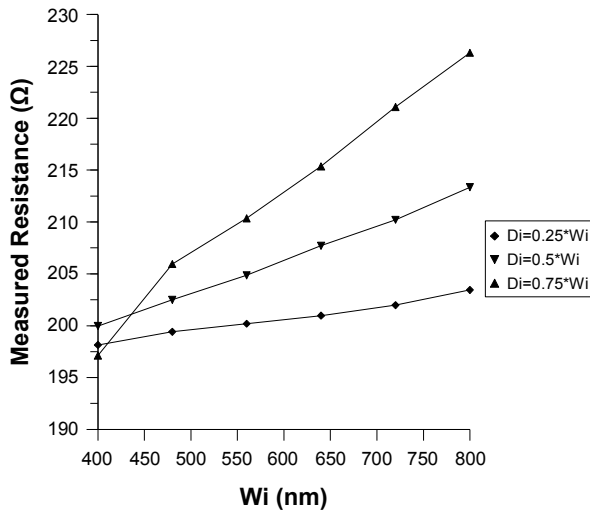
(a) Corner structures with CD=2000nm



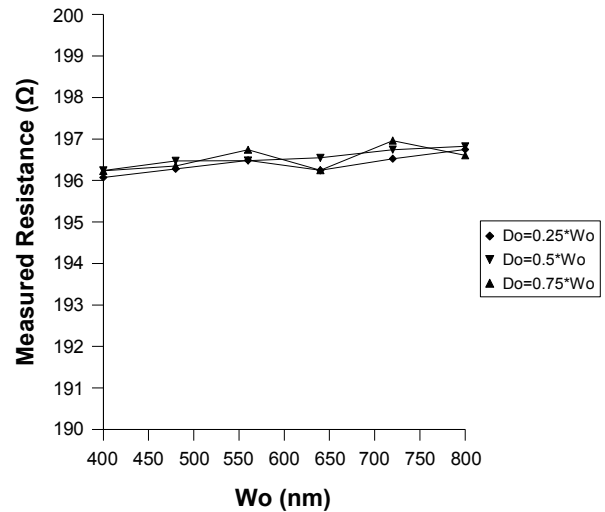
(b) Corner structures with CD=2400nm

Figure 5. Comparison of simulation results and on-mask measurements.

for 1600nm wide structures with OPC applied either to the inside or outside corner. As it was stated previously the electrical technique would be suited for detecting abnormalities on the fabricated serif features, particularly on inner corners. The resistance results of figure 6(a) follow the anticipated trends except for the structure with $D_i = 0.75 \times W_i$ and $W_i = 400\text{nm}$, where the resistance is smaller than normally expected. This is not a local mask effect as it can be seen in every structure with these inner serif dimensions, independent to their position on the mask and to the presence or absence of an outer serif. Therefore this is an indication that there is excess chrome at the area where a square of material should have been removed to form the inner serif. The deformed serif is most likely caused by the bridging of its two abutting corners, which they would nominally be in close proximity.



(a) Results of Changing Wi and Di



(b) Results of Changing Wo and Do

Figure 6. Electrical measurement results obtained from binary mask (MSN6754).

4.2. Optical Inspection

In order to visually investigate this effect a high-resolution Reichert Jung Polyvar optical microscope with Nomarski differential interference contrast optics was used to capture reflected light images of corner structures with and without the over-aggressive design dimensions. Figures 7(a) and 7(b) show the images of corner structures where $W_i = 400\text{nm}$, while $D_i = 0.25 \times W_i$ and $D_i = 0.75 \times W_i$ respectively. For $D_i = 0.75 \times W_i$ it appears that no chrome material has been removed from the area that forms the inner serif. For $D_i = 0.25 \times W_i$ although the design area that defines the inner serif is smaller than that of figure 7(b), it appears that the material has been removed. It is clear however, that the resolution of the images is inadequate and the optical tool is struggling to resolve the OPC features and thus clearly identify any difference between the structures. This confirms the problem of characterising advanced mask designs with OPC features, on conventional optical tools. Although mask features are usually four or five times larger than the printed dimensions, the OPC features are far smaller, similar to typical features on wafer level.

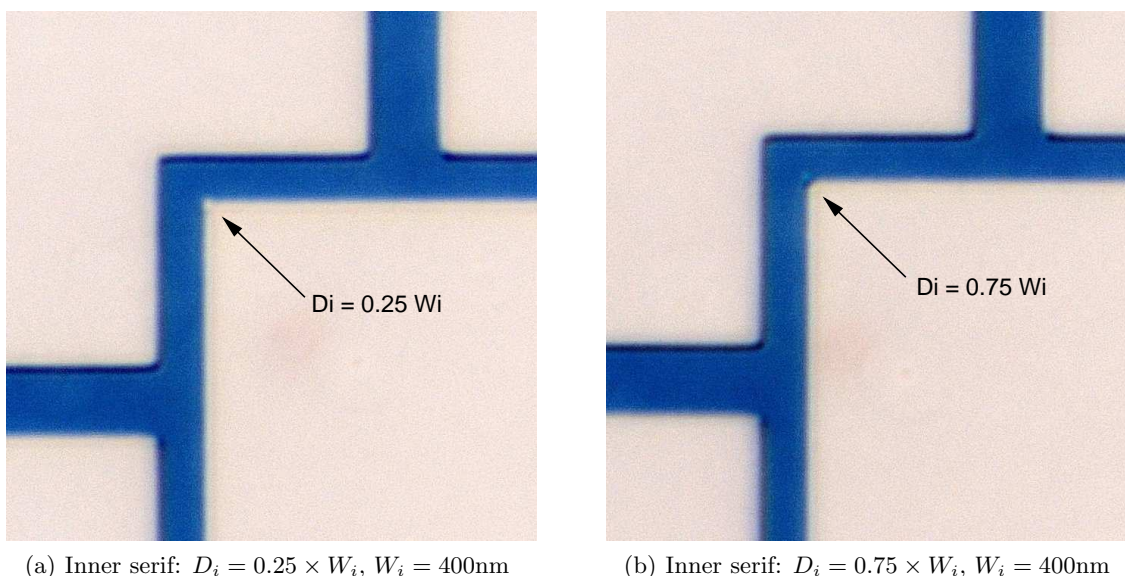


Figure 7. Optical images for corner structures with inner OPC features only.

Further optical images were obtained in transmitted light for the $W_i = 400\text{nm}$ features using a MueTec <M5k> mask metrology system operating with 248nm DUV illumination. These can be seen in figure 8 where (a) and (b) respectively show that inner corner serifs are defined for the $D_i = 0.25 \times W_i$ and $D_i = 0.5 \times W_i$ structures. Figure 8(c) reveals that there is no apparent modification to the $D_i = 0.75 \times W_i$ corner at all, consistent with an improperly formed (or missing) corner serif at this aggressive placement level. Other imaging techniques with better resolution are required in order to better understand the nature of the serif defect.

4.3. Atomic Force Microscope (AFM) Inspection

A Digital Instruments D5000 Atomic Force Microscope with superior resolution than the optical tools, was used to further investigate the reason for the change in resistance. The AFM scans cover the area surrounding the corner where the OPC features are located. The images of 1600nm wide structures with $D_i = 0.75 \times W_i$, $W_i = 0.25 \times \text{CD} = 400\text{nm}$ and $D_i = 0.75 \times W_i$, $W_i = 0.5 \times \text{CD} = 800\text{nm}$ can be seen in figures 9(a) and 9(b) respectively. Although there are outer OPC features also in these structures, the resistance values are similar to structures with no outer serifs. Differences in the resistance between structures with and without outer corner serifs are more likely to be caused by R_S , CD and inner corner rounding variations, rather than the actual presence or absence of an outer serif.

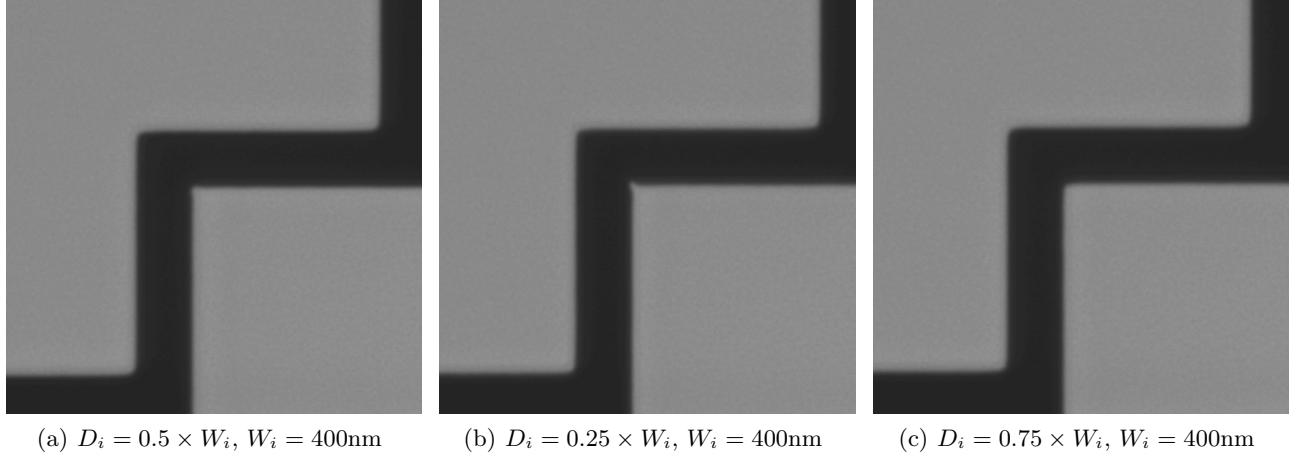


Figure 8. Optical images for structures with inner corner serifs.

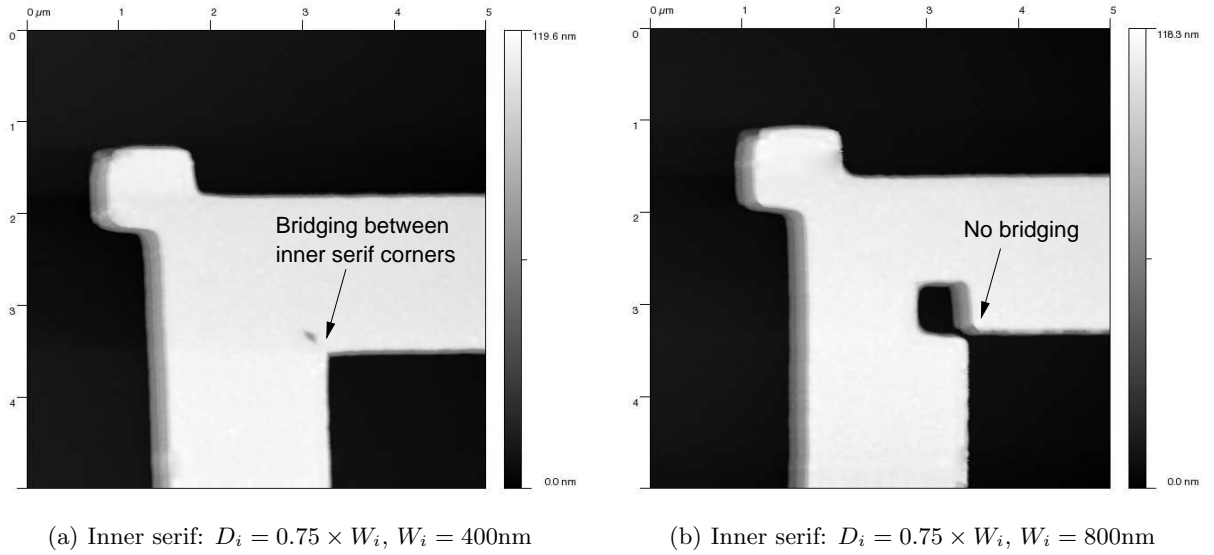


Figure 9. $5\mu\text{m} \times 5\mu\text{m}$ AFM scans of corner structures with inner and outer OPC features.

Figure 9(a) confirms that there is a problem with the fabrication of the inner serif for the specified dimensions. It appears that the spacing between the two neighbouring corners of the inner serif is too narrow to be resolved during fabrication. This causes the bridging of the two corners, which results in a very small partially processed area instead of a well defined inner serif. As this area is smaller than the diameter of the AFM tip, it is not possible to probe down to the surface of the quartz and assess properly the extent of the partial processing. Figure 9(b) shows the scan for an inner serif which retains the designed shape. Although the dimensions of this structure are larger, this is the desired effect as it will yield a well defined corner on the wafer.

4.4. Focused Ion Beam (FIB) Images

Another way of obtaining high resolution images is from a FIB mask repair tool. Figure 10 shows images of three progressively more aggressive corner serif offsets captured by a Seiko Instruments SIR 500 repair system, with the defective serif structure imaged in (c). This high resolution image indicates that the Cr layer is continuous at the serif location - the degree of offset is essentially too extreme for a feature of this size and the serif has detached itself from the line edge into a spot unresolvable by the lithography process. The electrical behaviour

of such a corner is more like that of an uncorrected one, albeit with a thinning of the Cr layer at the corner point. This is consistent with the measured resistance behaviour seen in figure 6(a).

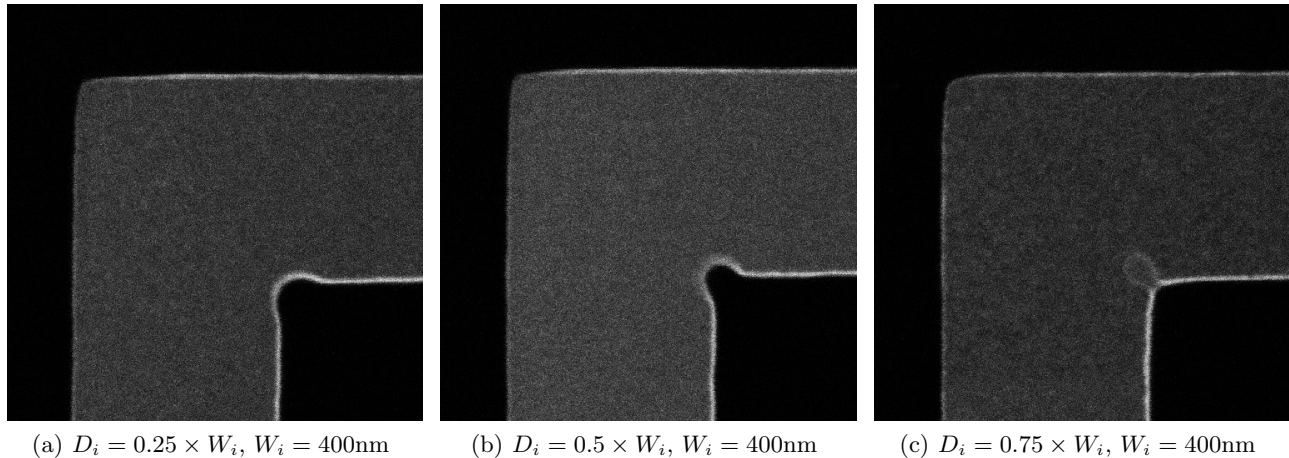


Figure 10. FIB images for structures with inner corner serifs.

5. CONCLUSIONS

This study has demonstrated the feasibility of extending electrical linewidth measurement techniques to the characterisation of two-dimensional OPC serif structures. Whilst restricted in practical application to inner corner serifs, it should be highlighted that it is this circuit feature that is most relevant to achieving designed device performance (and is indeed why it is sensitive to the described measurement technique in the first place). Inner corner serif structures are also the most notoriously difficult to manufacture and quantify using conventional optical metrology techniques.

The results from this work have clearly shown that electrical techniques are sensitive enough to measure the effects of small inner corner structures reliably and in good agreement with theoretical predictions. Any departures from the simulated results have been found to be attributable to defects in the serif structure. The agreement with simulation is a good indicator that it is the material physically present on the mask which is being characterised, removing some of the ambiguity inherent when interpreting indirectly acquired images of the mask pattern.

Future work will now be undertaken to correlate the measured resistance with actual serif area and how the offset between theoretical and measured values can be related to area loss arising from pattern fidelity of the rendered serif features. Structures on the test mask exist for wafer level measurements of corner structures to be made by the same electrical methods and it is hoped that these will form a valuable tool for investigating the quality of lithographic transfer and optimisation of inner corner serif structures.

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